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Planning

Supply of RFSoC based System-on-Module Electronic Boards

CERN

F01: Prior information notice
Prior information only
Notice identifier: 2024/S 000-037786
Procurement identifier (OCID): ocds-h6vhtk-04bdeb
Published 22 November 2024, 11:17am

Section I: Contracting authority

I.1) Name and addresses

CERN

CH – 1211 Geneva 23

Meryin

Contact

Hugh Alabaster

Email

hugh.alabaster@stfc.ukri.org

Country

United Kingdom

Region code

UK - United Kingdom

Internet address(es)

Main address

https://www.ukri.org/councils/stfc/

I.3) Communication

Additional information can be obtained from the above-mentioned address

I.4) Type of the contracting authority

European Institution/Agency or International Organisation

I.5) Main activity

General public services

Section II: Object

II.1) Scope of the procurement

II.1.1) Title

Supply of RFSoC based System-on-Module Electronic Boards

II.1.2) Main CPV code

- 31700000 - Electronic, electromechanical and electrotechnical supplies

II.1.3) Type of contract

Supplies

II.1.4) Short description

This Technical Description concerns the supply of 70 System-on-Module (SoM) electronic

boards with an AMD RF System-on-Chip (RFSoC) for the new signal acquisition and processing platform for the Beam Position Monitors (BPM) designed for the High-Luminosity Large Hadron Collider (HL-LHC).

II.1.5) Estimated total value

Value excluding VAT: 1,500,000 CHF

II.1.6) Information about lots

This contract is divided into lots: No

II.2) Description

II.2.2) Additional CPV code(s)

- 31220000 - Electrical circuit components
- 31710000 - Electronic equipment
- 31711000 - Electronic supplies
- 31712000 - Microelectronic machinery and apparatus and microsystems
- 31712114 - Integrated electronic circuits
- 31712300 - Printed circuits

II.2.3) Place of performance

NUTS codes

- UK - United Kingdom

II.2.4) Description of the procurement

CERN intends to place a Contract for the supply of 70 SoM electronic boards with an RFSoC (the “Supply”), as defined in this Technical Description and in accordance with the criteria defined in the Qualification Questionnaire. The Supply shall be a product already developed and commercialised by the Supplier, and not a new development. The Contract will be split into a pre-series phase (production of two units) and a series phase

(production of 68 units).

Technical Deliverables and Activities

The Supply shall include the following technical deliverables and activities:

• Pre-series (two units) and series (68 units) manufacturing of the electronic boards;

• An evaluation carrier board and open-source design examples to test the pre-series modules. The

design examples shall include, but not be limited to, system tests of both DDR memory sets, RF

clock configuration, ADCs and DACs performance;

• Technical documentation as listed in 5;

• Manufacturing documentation (detailed schematics, detailed Bill of Material (BOM), PCB

layout) of the SoM, as an option. The documents might be shared under an NDA or stored in an

escrow account managed by a third party to be accessed by CERN when the Supply is no longer

available for purchase by CERN;

• A description of the pin assignment of the RFSoC;

• A description of the pin assignment of the SoM connectors;

• Factory acceptance tests and associated documentation;

• A serial number associated with each SoM;

• Packing of the Supply;

• Shipping to CERN, if so requested;

• Technical support during the warranty period;

• Repair or replacement during the warranty period.

The SOM shall:

• be smaller than 120 x 150 mm;

• use an AMD Xilinx RFSoC, XCZU47DR or XCZU48DR, speed grade -1 or better, extended

temperature grade (E) or better, G1517 package;

• have dedicated separate DDR4 memories (each 4 GB or more) for the Processing System (PS)

and for the Programmable Logic (PL);

• have QSPI memory space for boot storage, with a minimum size of 128 MB;

• have the voltage regulation circuitry to generate all supply voltages required by the SoC and its

peripherals on the SoM; the voltages shall be generated from a supply voltage provided to the

SoM through one of the connectors;

• be capable of simultaneously using 8 ADCs running at 5 GSps and 8 DACs generating RF signals

of the maximum power at 10 GSps;

• have programmable circuitry to set the reference clocks for the SoC PS, for the GTR and GTY

transceivers and for the DDR memories;

• provide a connector-level separation of the analogue RF signals (ADC inputs and DAC outputs)

and other digital signals; the RF signals shall be routed as differential to a single board-to-board

multi-pin RF connector with controlled impedance; no analogue signal processing is allowed on

SoM;

• offer the possibility to provide the SoC with at least one programmable RF clock for the ADCs

and one RF clock for the DACs, either by on-board RF PLL system, or by the necessary pins on

the RF-side connector for off-board clock generation; in the latter case, a reference design of the

RF PLL circuitry to be implemented on the carrier board shall be provided;

• have the RF-side connector with additionally at least 8 pins connected to 8 lanes of a HD I/O

Bank of the SoC, available for application I/O;

• have the digital-side connector with at least 24 pins connected to 24 lanes of a HD I/O Bank of

the SoC, and at least 4 pins connected to 2 differential couples from a HP I/O Bank of the SoC,

available for application I/O;

• have the digital-side connector allowing the use of 4 PS transceivers GTR and at least 4 PL

transceivers GTY;

• have the digital-side connector allowing access to the UART interface of the PS;

• provide through the digital-side connector the possibility to reset the SoC and the SoM;

• be equipped with a factory-mounted heat spreader installed on the SoC supporting power loads

up to 50 W; the heat spread shall feature a mechanical

II.3) Estimated date of publication of contract notice

31 January 2025

Section IV. Procedure

IV.1) Description

IV.1.8) Information about the Government Procurement Agreement (GPA)

The procurement is covered by the Government Procurement Agreement: Yes

Section VI. Complementary information

VI.3) Additional information

Please note that even after the 'official' stated deadline on the market survey has passed, the contract remains open until the Invitation to Tender is issued. A Market Survey is merely an expression of interest and does not in any way constitute a commitment to bid. If you are interested in this contract, we encourage you to submit the Pre-Qualification Questionnaire and you are welcome to later decline if you decide you do not wish to proceed.